190 mu W at 10 MHz for F.O=3 and the maximum toggle frequency of 160 MHz were observed. The design of the VGC and experimental results for a device using 2 mu m design rules are described.

Classification Code

B1265B Logic circuits; B2570D CMOS integrated circuits; C5120 Logic and switching circuits

Controlled Indexing

CELLULAR ARRAYS; **CMOS** INTEGRATED CIRCUITS; INTEGRATED LOGIC CIRCUITS

Element Terms

W

Supplementary Indexing

gate delay 0.9 ns; power dissipation 190 microwatts; maximum toggle frequency 160 MHz; 2 micron design rules; Sharp; **variable gate width**; **sub-nanosecond bulk CMOS gate array**; loading capacitance; driving capability

Accession Number

1985:2528946 INSPEC

Session Cost: $5.26

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variable gate width AND

AND

cmos AND

AND

AND

AND

Date of publication of application — e.g.19980401 - 19980405

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Search History: May 24 13:36:16 2005

Search: gate width AND variable

Search: gate width AND variable AND cmos

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ANSWER 11

Title

Sharp applies **variable gate width** to design a sub-nanosecond bulk **CMOS gate** array.

Author

Torimaru, M.; Uratani, M.; Higashino, H.; Hondou, N.; Nakamura, T. (VLSI Res. Labs., Sharp Corp., Osaka, Japan)

Publication Source

AEU (March 1985) p.55-7. 4 refs.
CODEN: AEUNAX ISSN: 0385-0447

Document Type

Journal

Treatment Code

Practical; Experimental

Country of Publication

Japan

Language

English

Abstract

A sub-nanosecond bulk-**CMOS gate** array has been developed using a new basic cell approach VGC (**variable gate width** cell). Using the VGC, the loading capacitance of the **gate** can be reduced effectively and the driving capability can be increased. Thus, a **gate** delay of 0.9 ns for F.O=2, a power dissipation of